REMARKS

Claims 46-48, 51-56, 58-60, 62-65 and 67-91 are pending in this application. Claim 56 has been amended. Claims 61 and 66 have been canceled and their subject matter has been incorporated in amended independent claims 56 and 62, respectively. Claims 82-91 have been added to round out the scope of protection afforded by the present invention. No new matter has been introduced.

The drawings stand objected to under 37 C.F.R. § 1.83(a) for failing to show every feature of the invention specified in the claims. Specifically, the Examiner asserts that the drawings do not "show every feature of the invention specified in the claims." (Office Action at 2). In particular, the Examiner notes that the drawings must show "said devices" and "devices" as recited in claims 46, 56, 72, 75 and 76. (Office Action at 2). The drawings also stand objected to as "FIG. 1a-1f should be designated by a legend such as --Prior Art--." (Office Action at 2).

Applicants submit that the drawings show every feature of the invention specified in claims 46, 56, 72, 75 and 76. Applicants respectfully direct the Examiner's attention first to the first full paragraph on page 15 of the specification which states in part that "[s]ubsequent to the formation of the first pipe-shaped empty space 23, second pipe-shaped empty space 43, and plate-shaped empty space 53, additional interconnect structures and associated dielectric layers could be formed to create operative electrical paths down from the empty-spaced structures formed within the silicon substrate 10 and up to the silicon surfaces, such as the upper silicon surface 11, and any IC devices formed thereon." (Specification at 15). The text of the specification further emphasizes that "additional multilevel interconnect layers and associated dielectric layers could be formed to create operative electrical paths from the buried silicon structure 100 to a source/drain region (not shown) adjacent to a transistor gate structure (not shown) of the substrate 10. The substrate containing the buried conductors can be used in the formation of many types of integrated circuits such as memories, for example, DRAMs, processors etc." (Specification at 19, second full paragraph).

In addition, the "typical processor-based system 400 which includes a memory circuit 448, for example a DRAM, is illustrated in Figure 15. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory 448 communicates with the system over bus 452." The specification also specifies that "[m]emory 448, the CPU 444 or others of the illustrated electrical structures may be constructed as an integrated circuit, which includes one or more buried silicon structures 100 in accordance with the invention." (Specification at 19-20). Thus, the drawings illustrate that the device 446 over a bus 452 communicates with the memory 448 and with the system over bus 452.

A proposed drawing amendment for Figures 1a-1f is submitted for the Examiner's approval. Each of Figures 1a-1f is labeled -- Prior Art --.

Claims 56, 58 and 59 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamamoto et al. (U.S. Patent No. 5,963,838) ("Yamamoto"). This rejection is respectfully traversed.

The claimed invention relates to semiconductor devices and, in particular, to buried conductors within a substrate. As such, amended independent claim 56 recites a buried conductor pattern within a "monocrystalline substrate" comprising "at least one empty-spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration" and "a conductive material filling said empty space pattern such that at least a portion of a top surface of said conductive material is below a top surface of said monocrystalline substrate and at least a portion of a bottom surface of said conductive material is above a bottom surface of said monocrystalline substrate." Amended independent claim 56 further recites "said buried

conductor pattern forming at least a part of an interconnect between devices and being completely surrounded by monocrystalline material."

Yamamoto relates to a "transistor element . . . formed on the surface of a silicon substrate." (Abstract). According to Yamamoto, "[a] tunnel is formed in the silicon substrate at a position right under the transistor element" and "[a] contact hole is formed to extend from the surface of the silicon substrate to the contact hole." (Abstract). Yamamoto also teaches that "[s]ilicon oxide films are respectively formed on the inner surfaces of the tunnel and the contact hole" and that "[a] wiring layer is buried in the tunnel and the contact hole." (Abstract).

Yamamoto does not disclose all limitations of claims 56, 58 and 59. Yamamoto does not teach or suggest a "buried conductor pattern within a monocrystalline substrate," much less a "buried conductor pattern within a monocrystalline substrate" comprising "at least one empty-spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration," as amended independent claim 56 recites. Yamamoto teaches tunnel 30 which is "formed in the silicon substrate at a position right under the transistor element" and adjacent n-type well region 25, and not a "buried conductor pattern within a monocrystalline substrate," as in the claimed invention. In addition, Yamamoto does not disclose, teach or suggest a "buried conductor pattern forming at least a part of an interconnect between devices and being completely surrounded by monocrystalline material," as recited in amended independent claim 56 (emphasis added). For at least these reasons, Yamamoto fails to anticipate all limitations of amended independent claim 56, and withdrawal of the rejection of claims 56, 58 and 59 is respectfully requested.

Claims 46, 51, 52, 54, 55, 60, 72 and 75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Yamagata et al. (U.S. Patent No. 5,679,475) ("Yamagata") and Sato et al., *A New Substrate Engineering for the Formation of*

Empty Space in Silicon (ESS) Induced by Silicon Surface Migration, 1999 IEEE, pp. 517-20 ("Sato"). This rejection is respectfully traversed.

As noted above, the invention relates to semiconductor devices and, in particular, to buried conductors within a substrate. As such, independent claim 46 recites an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate." Independent claim 46 also recites that "at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate, said at least one buried conductor pattern having a spherical pattern and forming at least a part of an interconnect between devices." Independent claim 46 further recites "a conductive path extending from said buried conductor pattern to said devices."

Independent claims 72 and 75 recite "an integrated circuit substrate" comprising "at least one buried conductor pattern provided within a monocrystalline substrate such that at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate." Independent claim 72 further recites "said at least one buried conductor pattern having a plate-shaped pattern," whereas independent claim 75 further recites "said at least one buried conductor pattern having a pipe-shaped pattern."

Yamagata relates to a method of "preparing a semiconductor substrate" which comprises "a step of porousifying a silicon monocrystalline substrate to form a porous layer, a step of making a silicon monocrystalline thin film to epitaxially grow on a surface of the porous layer, a step of oxidizing the surface of the epitaxial growth layer, a step of forming a deposited film on the oxidized surface, thereby obtaining a first substrate, a step of closely contacting the deposited film of the first substrate to a second substrate, a step of heat treating the closely contacted substrates and a step of selectively etching the porous

layer." (Abstract).

Sato relates to a technique for forming empty spaces with various shapes in silicon substrates. Sato emphasizes that "[w]hen deeply-etched silicon substrates are annealed in a deoxidizing ambient, such as a hydrogen ambient, the silicon atoms on the surface migrate so as to minimize the surface energy." (Sato at 517). This way, for example, "trenches arranged in a row are transformed to an empty space shaped like a pipe, due to the combination of the grown empty spheres at the bottom of each trench." (Sato at 517).

The subject matter of claims 46, 51, 52, 54, 55, 60, 72 and 75 would not have been obvious over Yamamoto in view of Yamagata and Sato, whether considered alone or in combination. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996). Importantly, the teaching or suggestion to make the claimed combination and the reasonable expectation for success must both be found in the prior art and not based on the Applicants' disclosure. M.P.E.P. § 2142.

First, Yamamoto, Yamagata and Sato, whether considered alone or in combination, fail to teach or suggest a "buried conductor pattern" that forms "at least a part of an interconnect between devices," much less a "buried conductor pattern" that forms "at least a part of an interconnect between devices" and that is formed within "a monocrystalline substrate," as recited in independent claims 46, 56, 72 and 75. Yamamoto

in view of Yamagata and Sato, whether considered alone or in combination, also fail to teach or suggest a "buried conductor pattern" "forming at least a part of an interconnect between devices," as in the claimed invention.

Yamamoto fails to teach or suggest a "buried conductor pattern within a monocrystalline substrate," much less a "buried conductor pattern within a monocrystalline substrate" comprising "at least one empty-spaced pattern in said monocrystalline substrate," as in the claimed invention. Yamagata is silent about a buried conductor pattern, much less about a "buried conductor pattern" "forming at least a part of an interconnect between devices," as in the claimed invention. Sato is also silent about a "buried conductor pattern within a monocrystalline substrate," or about a "buried conductor pattern" "forming at least a part of an interconnect between devices," as in the claimed invention.

Second, a person of ordinary skill in the art would not have been motivated to combine the teachings of Yamamoto with those of Yamagata, as the Office Action asserts. On one hand, the crux of Yamamoto is a method of burying layers within a substrate to "prevent an increase in the number of wiring layers formed on a substrate." (Abstract). For this, Yamamoto teaches that "[a] tunnel is formed in the silicon substrate at a position right under the transistor element" and that "[a] contact hole is formed to extend from the surface of the silicon substrate to the contact hole." (Abstract). On the other hand, the crux of Yamagata is "a process for preparing an SOI semiconductor substrate by bonding." (Col. 1, lines 12-14). For this, Yamagata teaches "porousifying a silicon monocrystalline substrate to form a porous layer," "making a silicon monocrystalline thin film to epitaxially grow on a surface of the porous layer," "oxidizing the surface of the epitaxial growth layer, . . . forming a deposited film on the oxidized surface, thereby obtaining a first substrate, . . . closely contacting the deposited film of the first substrate to a second substrate, . . . heat treating the closely contacted substrates and a step of selectively etching the porous layer." (Abstract). Thus, Yamamoto and Yamagata do not even have in common the substrate on which their respective structures are formed. Accordingly, a person of ordinary skill in the

art would not have been motivated to combine the teachings of Yamamoto with those of Yamagata.

In addition, a person of ordinary skill in the art would not have been motivated to combine the teachings of Yamamoto with those of Sato. As noted above, the crux of Yamamoto is a method of burying layers within a substrate to "prevent an increase in the number of wiring layers formed on a substrate." (Abstract). Yamamoto teaches "implanting an impurity in a semiconductor substrate . . . to form an impurity-implanted layer in the semiconductor substrate, forming a contact hole extending from a surface of the semiconductor substrate and reaching the impurity-implanted layer, selectively etching the impurity-implanted layer to form a tunnel in the semiconductor substrate, and burying a conductive film in the tunnel and the contact hole." (Col. 6, lines 53-62). According to one embodiment of Yamamoto illustrated in Figures 32-38, "an oxygen-implanted layer 2 is formed in the silicon substrate 1 at a predetermined depth." (Col. 16, lines 49-50; Figure 32). At the time a field oxide film 3 is formed on the silicon substrate 1, "in the oxygen-implanted layer 2 . . . oxygen (O) is combined with silicon (Si) to form an SiO_2 layer 4." (Col. 16, lines 51-54; Figure 33). In contrast, Sato relates to empty space formation in a silicon substrate by drilling holes in the silicon substrate at a predefined depth, and then annealing the substrate at about 1100°C to form various empty space patterns. It is clear, therefore, that the only element which Yamamoto and Sato have in common is the silicon substrate in which their respective structures are formed. Accordingly, there is no motivation for a person of ordinary skill in the art to employ the Sato empty-space formation technique in the Yamamoto's method of forming an oxygen implanted layer and subsequently removing such layer.

In addition, Applicants note that courts have held that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." M.P.E.P. § 2143.01 (citing In re Ratti, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959). This is because the "suggested

combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which [the primary reference] construction was designed to operate." In re Ratti, 270 F.2d at 813, 123 U.S.P.Q. at 352.

In the present case, employing the empty space technique of Sato *in lieu* of the impurity implanting technique of Yamamoto, as the Office Action suggests, "would require a substantial *reconstruction* and *redesign* of the elements shown in [Yamamoto] (emphasis added)." Thus, the suggested combination of Sato and Yamamoto would have to eliminate the oxygen-implanted layer and the subsequently converted silicon dioxide layer of Yamamoto and, thus, redesign and reconstruct the elements of Yamamoto.

For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 46, 51, 52, 54, 55, 60, 72 and 75 is respectfully requested.

Claims 47, 48 and 76-81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Yamagata and Sato and in further view of Kenney (U.S. Patent No. 5,583,368). This rejection is respectfully traversed.

Independent claim 76 recites an "integrated circuit substrate comprising first and second buried conductor patterns provided within a monocrystalline substrate such that at least a portion of a top surface of each of said buried conductor patterns is below a top surface of said substrate and at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate." Independent claim 76 also recites "first and second buried conductive patterns forming at least a part of first and second interconnects between devices, respectively, wherein said first buried conductor pattern is located below said second buried conductor pattern and relative to said surface of said monocrystalline substrate." Independent claim 76 further recites "a first conductive path extending from said first buried conductor pattern and a second conductive path extending from said second buried conductor pattern."

Kenney relates to "[c]hips having subsurface structures within or adjacent a horizontal trench in bulk single crystal semiconductor." (Abstract). According to Kenney, "[s]tructures include three terminal devices, such as FETs and bipolar transistors, rectifying contacts, such as pn diodes and Schottky diodes, capacitors, and contacts to and connectors between devices." (Abstract). Kenney also teaches a "process for forming a horizontal trench exclusively in heavily doped p+ regions is presented in which porous silicon is first formed in the p+ regions and then the porous silicon is etched." (Abstract).

The subject matter of claims 47, 48 and 76-81 would not have been obvious over Yamamoto, Yamagata, Sato and Kenney. The cited references, whether considered alone or in combination, fail to teach or suggest all limitations of independent claims 46 and 76. None of Yamamoto, Yamagata, Sato and Kenney teaches or suggests a "buried conductor pattern *having a spherical pattern*," as independent claim 46 recites (emphasis added). Moreover, none of the cited references teaches or suggests "first and second buried conductor patterns provided within a monocrystalline substrate such that at least a portion of a top surface of each of said buried conductors pattern is below a top surface of said substrate and at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate," as independent claim 76 recites. For at least these reasons, the subject matter of claims 47, 48 and 76-81 would not have been obvious over Yamamoto, Yamagata, Sato and Kenney, and withdrawal of the rejection of these claims is respectfully requested.

Claims 62-64 and 67-71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Tsu et al. (U.S. Patent No. 6,294,420 B1) ("Tsu"). This rejection is respectfully traversed.

Amended independent claim 62 recites "a processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled

therein." Amended independent claim 62 also recites that the empty-spaced pattern has "one of a sphere-shaped, plate-shaped, or pipe-shaped configuration" and that "a conductive material" fills the empty space pattern "such that at least a portion of a top surface of said conductive material is below a top surface of said monocrystalline substrate and at least a portion of a bottom surface of said conductive material is above a bottom surface of said monocrystalline substrate, said conductive structure forming at least a part of an interconnect between devices and being completely surrounded by monocrystalline material."

Tsu relates to "an integrated circuit capacitor and a method of forming a capacitor." (Col. 1, lines 14-15). Tsu discloses that a capacitor may be used in a DRAM array, and that the memory array may be "embedded in a larger integrated circuit device." (Col. 7, lines 54-62; Col. 8, lines 61-67).

The subject matter of claims 62-64 and 67-71 would not have been obvious over Yamamoto and Tsu. Again, the Office Action fails to establish a *prima facie* case of obviousness. Yamamoto and Tsu, whether considered alone or in combination, fail to teach or suggest all limitations of amended independent claim 62. Yamamoto and Tsu fail to teach or suggest a "processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein," as amended independent claim 62 recites. Yamamoto and Tsu also fail to teach or suggest a buried conductive structure within a monocrystalline substrate, the conductive structure "forming at least a part of an interconnect between devices and being completely surrounded by monocrystalline material," as in the claimed invention.

In addition, a person of ordinary skill in the art would not have been motivated to combine the teachings of Yamamoto with those of Tsu. As noted above, the crux of Yamamoto is a method of burying layers within a substrate to "prevent an increase in the

number of wiring layers formed on a substrate." (Abstract). Yamamoto teaches "implanting an impurity in a semiconductor substrate . . . to form an impurity-implanted layer in the semiconductor substrate, forming a contact hole extending from a surface of the semiconductor substrate and reaching the impurity-implanted layer, selectively etching the impurity-implanted layer to form a tunnel in the semiconductor substrate, and burying a conductive film in the tunnel and the contact hole." (Col. 6, lines 53-62). On the other hand, Tsu teaches a "low resistance and low capacitance contact to subsurface electrodes . . . achieved by using highly conductive subsurface connectors which may be isolated by low dielectric insulator" to form "[s]tacks of devices are formed simultaneously within bulk single crystal semiconductor." (Abstract). Thus, again, the only structure which Yamamoto and Tsu have in common is their substrate on which their respective elements are formed. Accordingly, the disclosure of Tsu cannot supplement the inadequacies of Yamamoto, and withdrawal of the rejection of claims 62-64 and 67-71 is respectfully requested.

Claims 53, 65, 66, 73 and 74 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of various cited prior art references, including Sato, Tsu, Yamagata and Kenney. Applicants note that, as described above, the cited prior art references, whether considered alone or in combination, fail to teach or suggest all limitations of independent 46, 62 and 72. Accordingly, withdrawal of the rejection of claims 53, 65, 66, 73 and 74 is also respectfully requested.

Claims 82-91 have been added to round out the scope of protection afforded by the present invention. The newly added claims 82-91 recite a "buried conductive structure provided within a semiconductor substrate" formed *by inter alia* "forming at least one empty-spaced pattern beneath a surface of, and within a, semiconductor substrate, said empty-spaced pattern being surrounded by semiconductor material" and "forming at least one opening within said semiconductor substrate, said opening connecting a respective empty-spaced pattern with the exterior of said semiconductor substrate." Newly added claims 82-91 also recite "forming a conductive material in said empty-spaced pattern and

said opening." Applicants submit that none of the cited prior art references teaches or suggests all limitations of newly added claims 82-91.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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